NVM as a Disruptive Technology

#OFADevWorkshop
Non-Volatile Memory Vision

Fast Like Memory

Durable Like Storage

NVM Brings Storage

Make Data Durable Without Doing IO!
Next Generation Scalable NVM

Resistive RAM NVM Options

<table>
<thead>
<tr>
<th>Family</th>
<th>Defining Switching Characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase Change Memory</td>
<td>Energy (heat) converts material between crystalline (conductive) and amorphous (resistive) phases</td>
</tr>
<tr>
<td>Magnetic Tunnel Junction (MTJ)</td>
<td>Switching of magnetic resistive layer by spin-polarized electrons</td>
</tr>
<tr>
<td>Electrochemical Cells (ECM)</td>
<td>Formation / dissolution of “nano-bridge” by electrochemistry</td>
</tr>
<tr>
<td>Binary Oxide Filament Cells</td>
<td>Reversible filament formation by Oxidation-Reduction</td>
</tr>
<tr>
<td>Interfacial Switching</td>
<td>Oxygen vacancy drift diffusion induced barrier modulation</td>
</tr>
</tbody>
</table>

Scalable Resistive Memory Element

Cross Point Array in Backend Layers

~ 1000x speed-up over NAND.

From Jim Pappas, Intel, SNIA NVM Summit
Merging Storage and Memory

Role-sharing Positioning of Emerging Research Memories

- High-Speed eSRAM
- STT-RAM
- ReRAM
- eSRAM
- eDRAM
- eFeRAM
- DRAM
- eFlash
- NOR-Flash
- NAND-Flash

Clock Frequency (Hz)
- 1G
- 100M
- 10M

Cell Area (μm²)
- 100
- 50
- 10
- 5
- 1

Applications:
- High-speed Graphics: Games
- High-density work memory: PC
- High-speed MCU: Car
- Parameter storage: IC tag / smart-card
- Program storage: Mobile phone, PDA
- Data storage: DSC, SSD, USB memory
- Low-power work memory: Mobile phone
- Front-end SoC: ASSP, ASIC
- High-speed MPU: Supercomputer

From Ed Grochowski, 2014 Report on New Storage Technologies
Storage Latency is Changing

SSD Latency Profile – In the next generation, media is not the bottleneck.

From Jim Pappas, Intel, SNIA NVM Summit
Interconnect and Software Will Soon Dominate Latency

Application to SSD IO Read Latency (us, QD=1, 4KB)

- NAND MLC SATA 3 ONFI 2
- NAND MLC SATA 3 ONFI 3
- NAND MLC PCIe Gen 3 ONFI 3
- Future NVM PCIe x4 Gen 3

From Jim Pappas, Intel, SNIA NVM Summit
Opportunities with Next Generation NVM

NVM Express/SCSI Express: Optimized storage interconnect & driver
SNIA NVM Programming TWG: Optimized system & application software

From Jim Pappas, Intel, SNIA NVM Summit
Software overheads are being driven to keep pace with devices. NUMA latencies up to 200 nS have historically been tolerated. Anything above 2-3 μS will probably need to context switch. Latencies below these thresholds cause disruption.
Memory Disaggregation

Increased flexibility to provision memory from a shared pool
Pass data or VM’s between servers without moving bits
Enabled at rack scale using silicon photonics
Application View of Memory Properties

Durability
• Applications should know which memory is persistent.

NUMA
• What part of the system manages proximity of processing to memory?
  • How much unpredictability is tolerable?

Multi-processing
• SMP boundaries implied by distance and fault domains
Abstractions need to account for...

**Resource Diversity**

- Choosing the right memory resources in real time

**System Scalability**

- Programming model accounts for wide scale

**Transactions**

- Accelerate recoverability to memory speed
Thriving in Chaos

• Make sure hierarchy levels earn their places

• Think dual stack

• Make middleware take up the slack

• Mind the fault lines
Thank You