Criteria for a Scalable Architecture

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Exascale Systems Challenges are both Interconnect and SAN

• Design with system focus that enables end-user applications

• Scalable hardware
  – Simple, Hierarchal
  – New storage hierarchy with NVRAM

• Scalable Software
  – Factor and solve
  – Hierarchal with function shipping

• Scalable Apps
  – Asynchronous coms and IO
  – In-situ, in-transit and post processing/visualization
Myth: Moore’s Law is dead!
Reality - Moore’s Law is Alive and Well

The foundation for all computing
LINPAC Performance 2x/1yr CAGR

Performance CAGR driven in part by geometric increase in node counts. Technology in TOP10 impacts entire TOP500 in 6-8 years.

Slide courtesy Jack Dongarra
Tera→Peta-Scale trends are not sustainable

<table>
<thead>
<tr>
<th>System</th>
<th>date</th>
<th>peak</th>
<th>nodes</th>
<th>cores</th>
<th>power</th>
<th>Facilities Impact</th>
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<tr>
<td>BluePacific ID</td>
<td>1996</td>
<td>0.14</td>
<td>512</td>
<td>512</td>
<td>0.13</td>
<td>B113 Air Handler</td>
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<td>BluePacific TR</td>
<td>1997</td>
<td>1.81</td>
<td>674</td>
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<td>BluePacific SST</td>
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<td>3.90</td>
<td>1,452</td>
<td>5,808</td>
<td>0.43</td>
<td>B113 2x to 1.8MW</td>
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<td>1.00</td>
<td>B451 2x to 3.9MW</td>
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<td>BlueGene/L</td>
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<td>Purple</td>
<td>2005</td>
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<td>1,536</td>
<td>12,288</td>
<td>4.80</td>
<td>New Building 3x</td>
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<td>Dawn</td>
<td>2009</td>
<td>501.35</td>
<td>36,864</td>
<td>147,456</td>
<td>1.15</td>
<td></td>
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<tr>
<td>Sequoia</td>
<td>2011</td>
<td>20,133</td>
<td>98,304</td>
<td>1,572,864</td>
<td>8.00</td>
<td>B453 2x to 30MW</td>
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</table>
Where technology will get us...

• First: Continued advances in silicon technology...
  - 2x density every generation. This is half of the story as we have a new silicon generation ~ 2 years.
  - The other factor of 2 every two years has come in through increasing levels of integration and architectural discontinuities.
    - In reality progress is comprised of “evolutionary” curves on top of discontinuous architectural change. Expect another discontinuity around exascale as evolutionary many-core will start to fall off the curve.

• Fundamental changes in memory technology will change the I/O story through integrated NVM
Dealing With Power and Scaling Issues

Low voltage puts pressure on intra-process scaling and cost

Two key areas of integration are next...

• Memory:
  - New bandwidth/density ratio. Needed to compensate for compute increasing faster than DRAM density. Does fundamentally change the game.
    - Bandwidth is more fundamental than density.
  - New technologies are nearing prime time. Could fundamentally change the game.

• Network:
  - Time to integrate.
    - Performance, cost and power all contribute.
The Memory Challenge to Exascale

Memory Bandwidth and Capacity

- Relative Growth in Mem BW
- # of cores
- Flops/cycle/Socket
- Expon. (Required Memory BW)

Peak Performance of some of the most recent Top 10 machines

1 Byte/Flop
0.1 Byte/Flop
0.01 Byte/Flop
0.001 Byte/Flop

Peak Performance (TF)
Memory (TB)
This was a useful metric before compute got cheap and vector units proliferated.

- Fundamentally this is the ratio of a very expensive resource divided by a very inexpensive resource.
- 1.0 B:F for scalar floating (FMA included) still looks right.
- This metric gets confused on wide vectors (need full scatter gather to get broad multiplicativ performance impact).
- Cache blocking for codes that get high fraction of peak reduces the main memory bandwidth requirements.
- Yes more is better.
Barriers to innovations sometimes come from the past..

- There are a number of metrics which are commonly used but often not meaningful without context. Need to remove barriers to innovation driven by adherence to legacy metrics.
  - B:F at main store? (which flops?)
  - B:F at network?
  - Memory/core? (threading makes this very weak)
  - Perf/Socket?
  - What is our measure of the goodness of a machine?
Re-think DRAM Architectures

Today’s DRAM
- Activates one large page
- Lots of reads and writes (refresh)
- Small amount of read data is used
- Power wasted in maintaining/accessing the array

Revised DRAM
- Activates one smaller page
- Fewer Read and write (refresh)
- Most of the read data is used
- IO can be widened to increase BW
Innovative Packaging & IO Solutions

Pins required + IO Power limits the use of traditional packaging

Tighter integration between memory and CPU

High BW and low latency using memory locality

The Advantages of Fabrics Integration

Problem:
- **Power** – System IO Interface Adds “10s Of Watts” Incremental Power
- **Cost & Density** – More Components On A Server Node
- **Scalability** – Processor Capacity & Fabric Bandwidth Scaling Faster Than System IO Bandwidth

Solution:
- Removing The System IO Interface From The Fabrics Solution **Reducing Power**
- An Integrated Fabrics Results In **Fewer Components On The Server Node**
- An Integrated Fabric **Balances Fabric and Compute, Scaling Application Performance & Efficiency**

Fabrics Integration Required to Scale Performance & Power
Silicon Photonics

A game changer for long links => Reduces power, latency, and cost
Data delivery over large distances with no EMI effects and high wiring density
Current research shows data transmission rates of >10Gb/s

Si Photonics is the Only Solution for Long Links
Weak Scaling Zrad3D – 3D Radiation problem’s average zone-iteration grind time per machine

- Purple at Retire (NewComm)
- Dawn - 2.2
- Sierra - Full QDR
- Muir - Full QDR
- Cielo - PGI Full (16 MPI/Node)
- Zin - Full (16 MPI/Node)

Slopes:
- 0.000079 Purple
- 0.000016 Dawn (BG/P)
- 0.000012 Zin
- 0.000010 Cielo
- 0.000008 Sierra
- 0.000005 Muir

Note: 0 slope is ideal scaling
**Weak Scaling Zrad3D - 3D Radiation problem’s average zone-iteration grind time per machine**

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QDR-40/SeaStar2+

From: Unprecedented Scalability and Performance of the NNSA Tri-Lab Linux Capacity Cluster 2
Summary

- Integration of memory and network into processor will help keep us on the path to Exascale
- Energy is the overwhelming challenge. We need a balanced attack that optimizes energy under real user conditions
- B:F and memory/core while they have their place, they can also result in impediments to progress
- Commodity interconnect can deliver scalability through improvements in Bandwidth, Latency and message rates
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