



OPENFABRICS  
ALLIANCE

14<sup>th</sup> ANNUAL WORKSHOP 2018

# INTEL® OMNI-PATH ARCHITECTURE AND NVIDIA GPU SUPPORT

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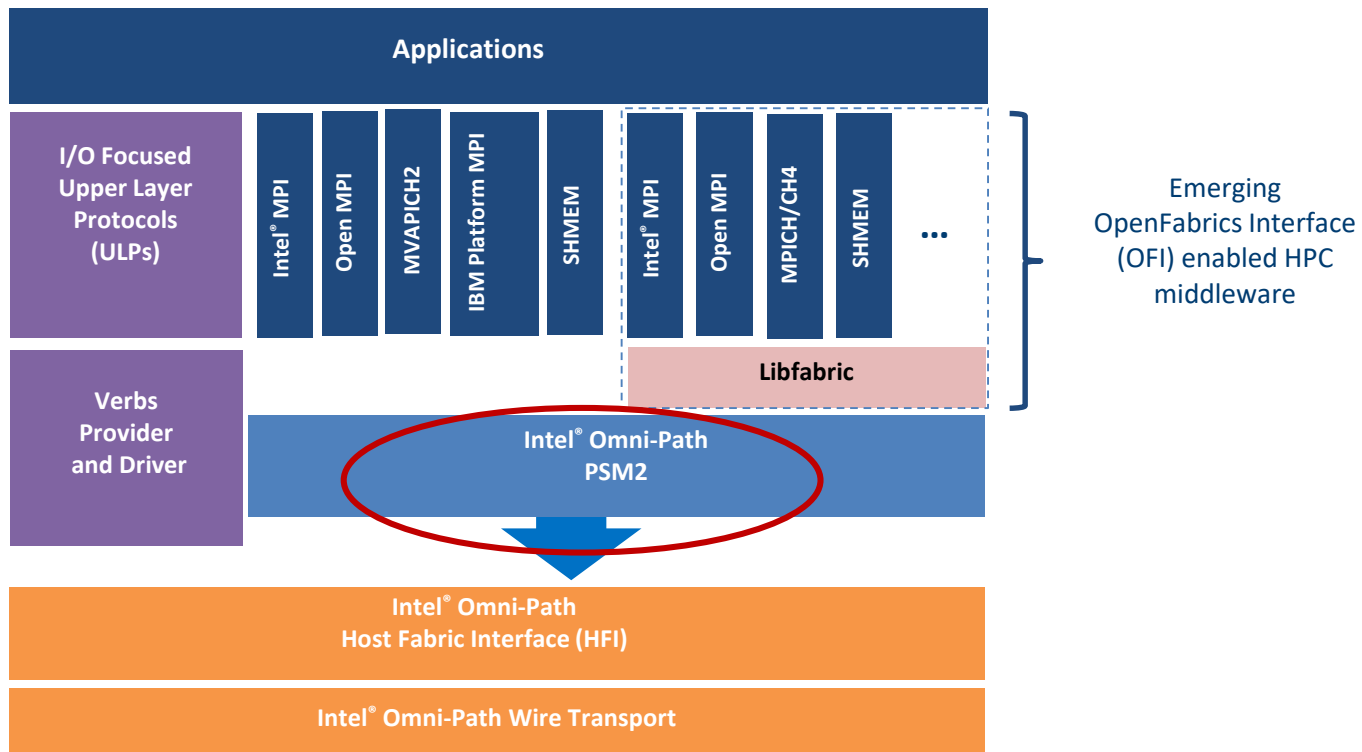
[ April, 2018 ]



# INTEL® OMNI-PATH ARCHITECTURE HPC

## DESIGN FOCUS ARCHITECTED FOR YOUR MPI APPLICATION

Designed for Performance at Extreme Scale

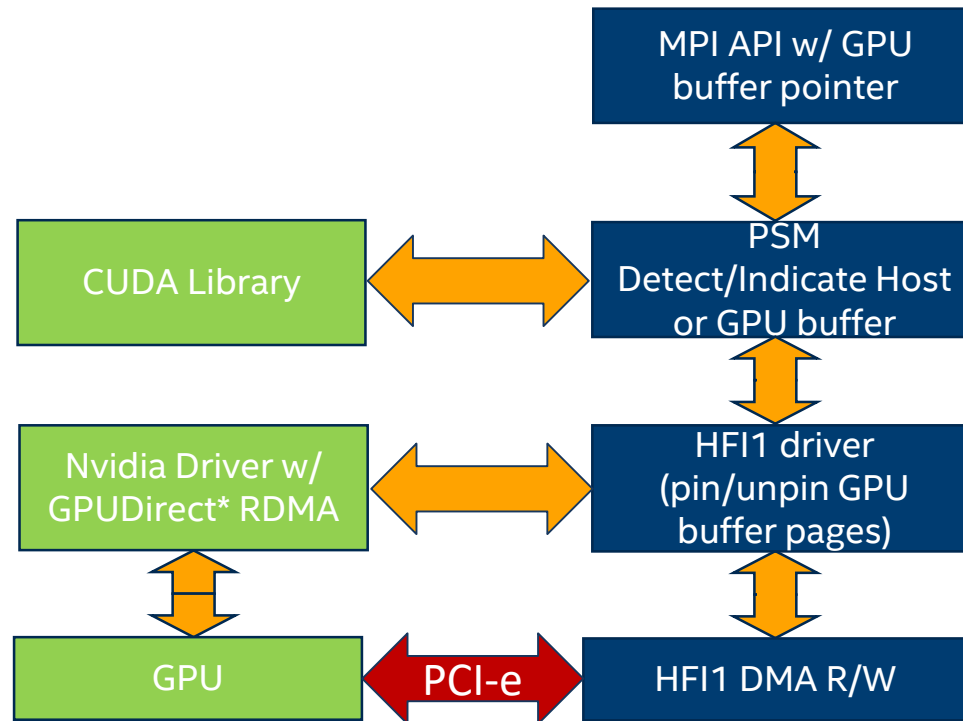


# PSM2

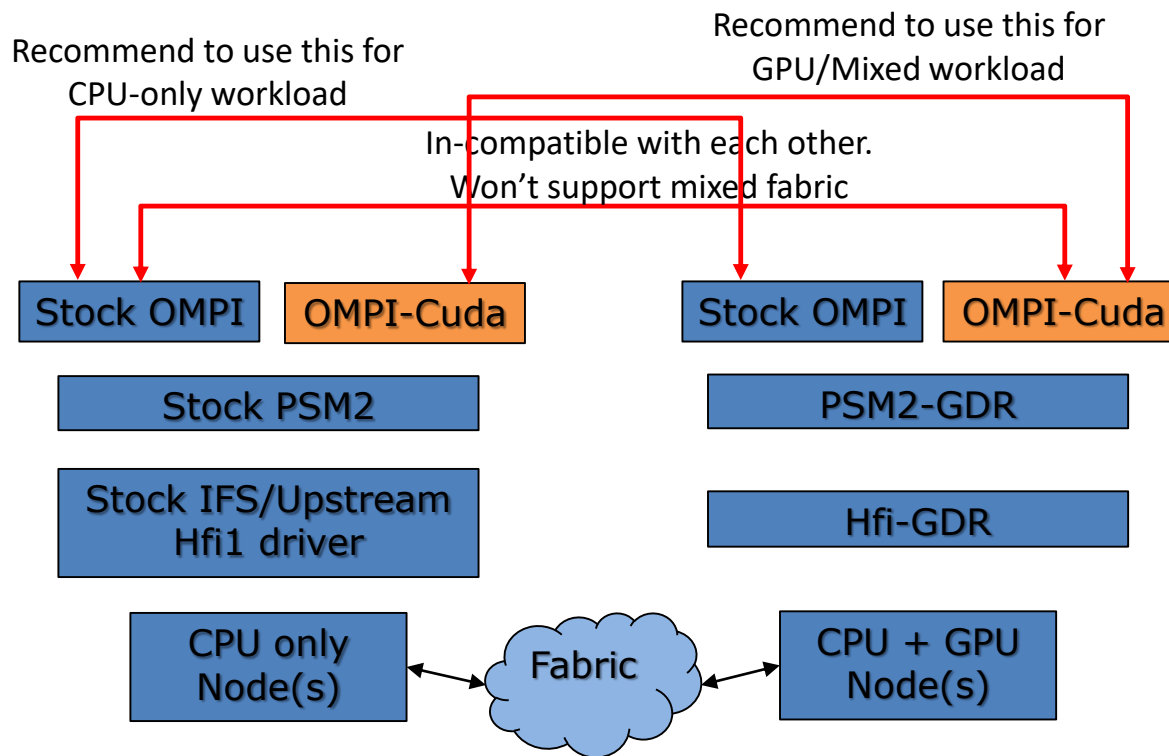
- PSM2 API is a low level high performing communication interface
- Semantics matches with that of compute middleware such as MPI and/or OFI
- PSM2 EP maps to HW context, Each EP associated with matched queue
- API's are optimized for both latency and bandwidth
- PIO/Eager for small message latency
- DMA/Expected for optimal Bandwidth with large message size
- Intel MPI, Open MPI and MVAPICH2 use PSM2 transport for Omni-Path Fabric
- PSM2 Programmer's Guide available @ [https://www.intel.com/content/dam/support/us/en/documents/network-and-i-o/fabric-products/Intel\\_PSM2\\_PG\\_H76473\\_v8\\_0.pdf](https://www.intel.com/content/dam/support/us/en/documents/network-and-i-o/fabric-products/Intel_PSM2_PG_H76473_v8_0.pdf)



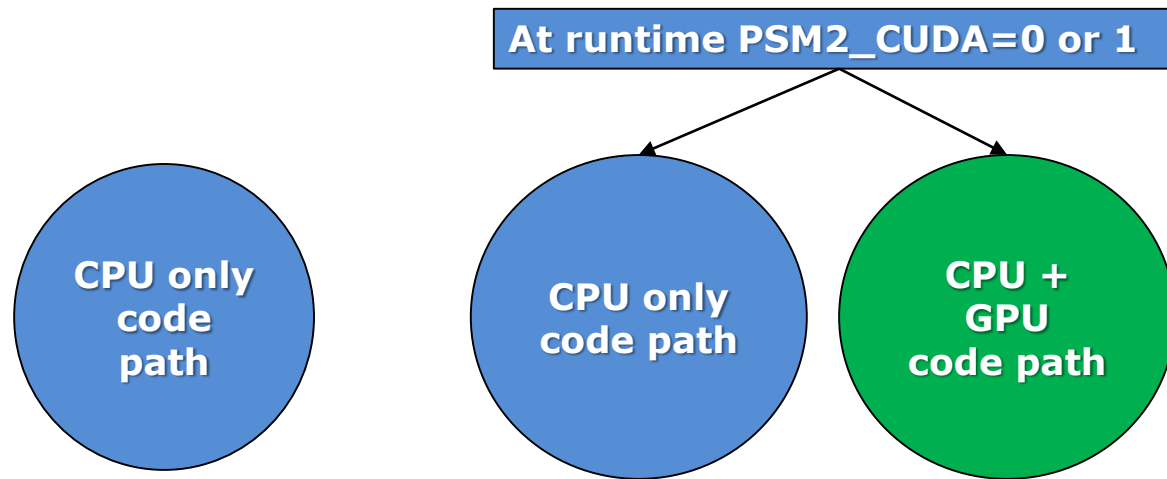
# SIMPLISTIC HIGH-LEVEL VIEW OF OPA + GPU STACK



# OPEN MPI STACK VIEW



# PSM2 CODE STRUCTURE



Single Source in GITHUB to build CPU or CPU + GPU binary

# RUNNING MPI WORKLOADS

- **PSM2 level runtime ENV vars to mpirun**
  - **GPU Workloads**
    - Set PSM2\_CUDA=1
      - Enable cuda code path at runtime
    - Set PSM2\_GPUDIRECT=1
      - Enable GPUDirect\* RDMA technology
    - PSM2\_GDRCPY=1 by default when PSM2\_GPUDIRECT=1
      - Enables low latency transfers for small messages
  - **CPU-only workloads:** default values, no need to set the variables
    - PSM2\_CUDA=0
    - PSM2\_GPUDIRECT=0
- **Example using CUDA-aware Open MPI**
  - `mpirun -np 2 --map-by ppr:1:node -host host1,host2 -x PSM2_CUDA=1 -x PSM2_GPUDIRECT=1 -x HFI_UNIT=1 ./osu_latency -d cuda D D`



# PSM2 GPU PLATFORM SPECIFIC TUNING

- **Defaults are expected to be optimal in most cases**
- **PSM2\_GDR\_COPY\_SEND\_THRESH (32 bytes)**
  - Send side threshold for GDR Copy, above this limit uses GPUDirect technology
- **PSM2\_GDR\_COPY\_RECV\_THRESH (64000 bytes)**
  - Send side threshold for GDR Copy, above this uses GPUDirect technology
- **PSM2\_GPUDIRECT\_SEND\_THRESH (30000 bytes)**
  - Above this threshold switch to 2MB window pipeline sends through the host
- **PSM2\_GPUDIRECT\_RECV\_THRESH (UINT\_MAX)**
  - Above this threshold switch to 2MB window pipeline receives through the host
  - Default assumes both OPA and GPU are on the same CPU socket
  - Set this variable when both OPA and GPU are connected to different sockets



# PSM2 NUMA AWARENESS

- **PSM2 Device Selection algorithm**
  - Combination of first and best fit algorithms
    - Find all active OPA devices (units) in system.
    - If only one device found then return and use this device for all communication
  - Scan for OPA devices that are on same NUMA node(root complex)
    - Uniformly distribute the process among the OPA devices found
    - If no devices are found in current NUMA node, then select OPA device from remote NUMA node.

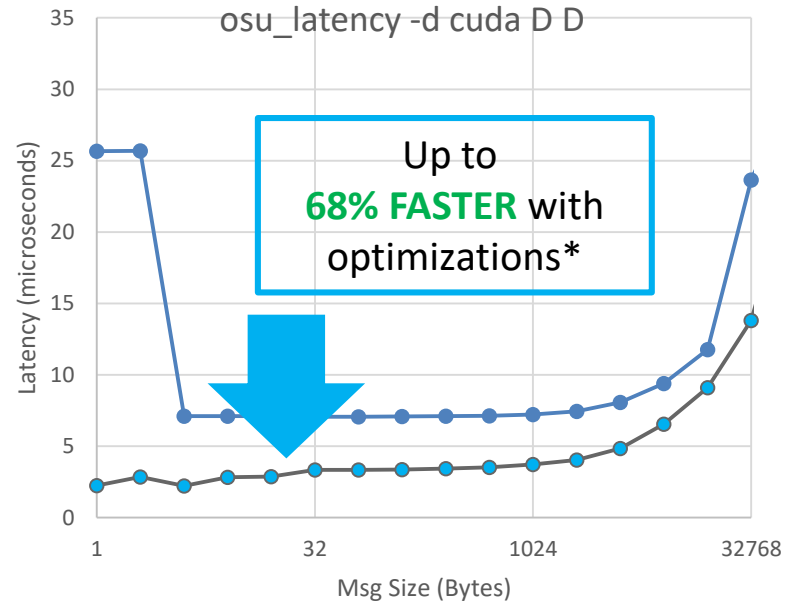
*Ravindra Babu Ganapathi ; Aravind Gopalakrishnan ; Russell W. McGuire, MPI Process and Network Device Affinitization for Optimal HPC Application Performance, High-Performance Interconnects (HOTI), 2017*

# OPEN MPI ENABLING

- **Open MPI handles GPU Buffers when built with CUDA Support**
- **Converter flag added specific to PSM2 MTL**
  - Indicates PSM2 support for GPUDirect\* to OPAL layer
  - Flag allows OPAL layer to skip CUDA convertor set up phase
  - Facilitates to bypass CUDA transfers in OPAL for contiguous MPI data-types
  - PSM2 automatically handles all GPU buffers
- **PSM2 handles all pt2pt and blocking collectives**
- **Open MPI continues to handle non-contiguous MPI data-types**
  - Pack/Unpack datatypes into contiguous memory before transfers
- **Open MPI Upstream info**
  - Enabled Open MPI branches v2.x, v3.0.x, v3.1.x to support OPA + GPU
  - Version 2.1.3 released with this feature (released 03/15/18)
  - Upcoming versions v3.1.0, v3.0.1 will also have the feature (currently both are release candidates)

# GPU BUFFER TRANSFER LATENCY - UPCOMING INTEL® OPA OPTIMIZATIONS

## NVIDIA\* CORPORATION TESLA P100\*



— Baseline

— IFS 10.7 Optimized

Intel® Xeon® processor E5-2699 v4, SLES 12.3 4.4.73-5-default, 0xb00001b microcode. Intel Turbo Boost Technology enabled. Dual socket servers connected back to back with no switch hop. NVIDIA\* P100 and Intel® OPA HFI both connected to second CPU socket. 64GB DDR4 memory per node, 2133MHz.

OSU Microbenchmarks version 5.3.2 Open MPI 2.1.2-cuda-hfi as packaged with IFS 10.7.

\* 68% higher claim based on 4 byte latency \*\* 30% higher claim based on 8KB uni-directional bandwidth. 73% higher claim based on 64B bi-directional bandwidth.

Optimized performance: mpirun -np 2 --map-by ppr:1:node -host host1,host2 -x PSM2\_CUDA=1 -x PSM2\_GPUDIRECT=1 -x HFI\_UNIT=1 ./osu\_latency -d cuda D D

Baseline performance: same as above but with "-x PSM2\_GDRCPY=0 (off)"

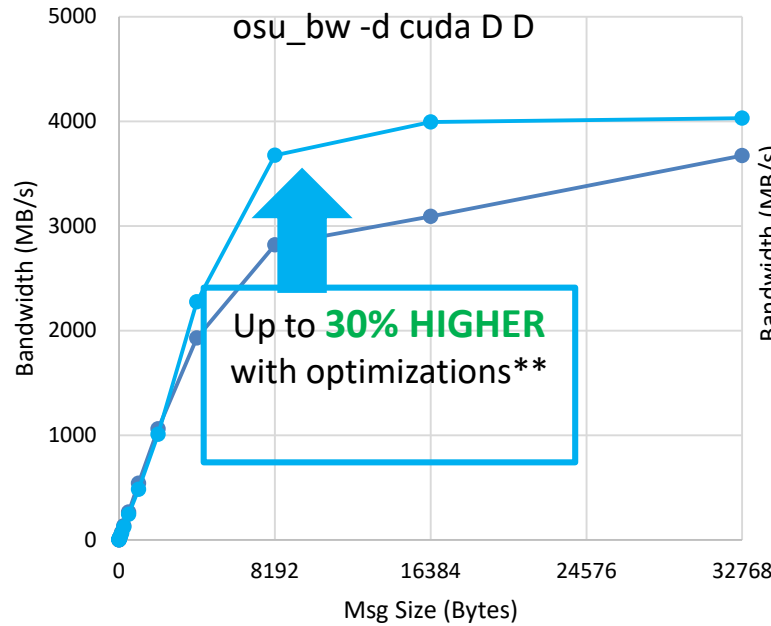
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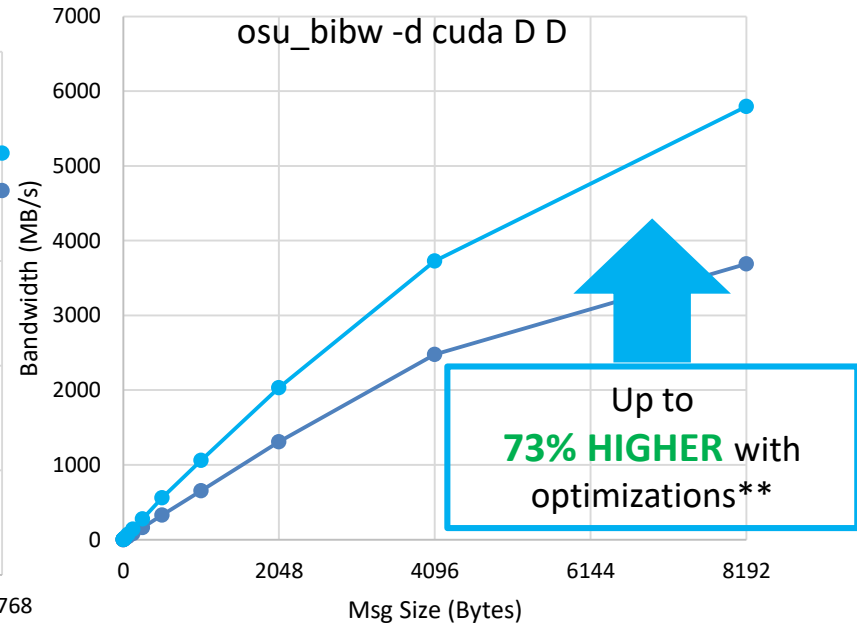
# GPU BUFFER TRANSFER BANDWIDTH - UPCOMING INTEL® OPA OPTIMIZATIONS

## NVIDIA\* CORPORATION TESLA P100\*

### Uni-dir Bandwidth



### Bi-dir Bandwidth



— Baseline

— IFS 10.7 Optimized

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Baseline performance: same as above but with `"-x PSM2_GDRCPY=0 (off)"`

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**THANK YOU**

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